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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,055	12/31/2001	James K. Falbo	NTI-030	1929

29477 7590 09/09/2005

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/040,055
Filing Date: December 31, 2001
Appellant(s): FALBO ET AL.

Jeanette S. Harms
For Appellants

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06/20/2005.

(1) Real Party in Interest

A statement identifying the real party in interest as Synopsys Inc. is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The Appellants' statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The Appellants' statement of the ground of rejection is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

6,523,162 AGRAWAL et al. 02-2003

(9) Grounds of Rejection

The following ground of rejection is applicable to the appealed claims:

Claims 11, 33, 37-43, 55-99 are finally rejected under 35 U.S.C. § 102(e) as being anticipated by Agrawal et al. (US Patent 6,523,162). The final rejection is set forth in a prior Office Action, mailed on 03/11/2005. Independent claims 11, 33, 72 and 96 are representative and are reproduced below along with corresponding citations from Agrawal et al. used for rejection of the limitations of the claims 11, 33, 72 and 96.

Claim 11	
A method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons	column 14, lines16-19; column 5, lines 51-52; column 8, lines.45-48
the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout	column 14, line 31 column 14, lines 24-30
the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection	column 14, lines 20-23
the second edge being contiguous with and substantially perpendicular to the first edge	column 6, lines 35-37 as shown on the Figures 4a, 4b and 4c which provide examples of basic shapes
and wherein the first shape further comprises: a third edge, the third edge being contiguous with and substantially perpendicular to the second edge	as shown on the Figures 4a-4c, 5a-5d, 6a-6e, 7a-7c and particularly according the Figure 4b
a fourth edge, the fourth edge being contiguous with and substantially perpendicular to the third edge	as shown o the Figures 4a-4c, 5a-5d, 6a-6e, 7a-7c and particularly according the Figure 4c wherein the fourth edge E434 is contiguous and substantially perpendicular with the third edge E433;

and a fifth edge, the fifth edge being contiguous with and substantially perpendicular to the fourth edge, wherein none of the first edge, the second edge, the third edge, the fourth edge, and the fifth edge are substantially side-by-side with each other	column 6, lines 44-51; column 17, lines 10-21; as shown on the Figures 4a-4c, 5a-5d, 6a-6e, 7a-7c and particularly according the Figure 4c wherein the fifth edge E435 is contiguous and substantially perpendicular with the fourth edge E434

Claim 33	
A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features	column 19, lines 25-26; column 20, lines 1-2
the software program comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property	column 20, lines 3-7; lines 20-23
a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features	column 20, lines 24-25
third set of instructions for defining the first shape according to a set of user inputs	abstract; column 20, lines 20-22

Claim 72	
A system for performing layout beautification on an integrated circuit (IC) layout data file	Figure 10a; column 12, lines 17-18; lines 21-22
the system comprising: an input data manager for loading the IC layout data file into the system	Figure 10a; column 12, line19
a layout beautification engine for applying a plurality of corrective actions to the IC layout data file responsive to at least one of a plurality of shapes associated with each of the plurality of corrective actions matching elements in the IC layout data file, wherein each of the plurality of shapes comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties	Figure 10b; column 12, lines 49-50; column 12, lines 51-60

and output data manager for generating an output data file	Figure 10a; column 12, lines 20-21

Claim 96	
A shape-based beautification method in a layout	column 14, lines 16-19; column 5, lines 51-52; column 8, lines 45-48
the method comprising: identifying a shape pattern on the layout	column 14, lines 20-23
and applying at least one of an absolute correction, an adaptive correction and a replacement correction to the identified shape pattern,	column 4, lines 49-50; column 4, lines 45-48
thereby removing at least one layout imperfection and reducing fracturing data volume in the layout	column 8, lines 45-48; column 12, lines 31-37; lines 41-44; column 11, lines 35-36; column 10, lines 64-67

(10) Response to Argument

Introduction

It has to be noted, that the claims to Layout Beautification method (operation) contain a **non-limiting preamble.** Independent claim 11, 79, 89 and 96 contain "Layout beautification method/operation" as a preamble when the following body of the claims is a self-contained description of the structure (steps) and does not depend on the preamble for completeness. So the preamble does not limit the claim. Agrawal et al. discloses all steps represented by the limitations of the independent claims 11, 79, 89 and 96 and read into them, since claimed steps do not recite layout beautification or layout imperfections (independent claim 65) (see ***IMS Technology v. HAAS Automation INC.*, 54 USPQ2d 1129, 1137 (Fed. Cir. 2000)**).

Further, paragraphs [006], [0015], [0009] and [0082] of Appellants' Specification disclose Layout Beautification method/operations without specifying the actual steps of Layout beautification **to distinguish it from optical proximity correction (OPC) modification and design rule checking (DRC)**. Therefore, Layout Beautification method/operations as claimed and described in specification is satisfied by Agrawal et al.

With respect to claims 33, 37, 38, 39, 40, 55, 72, 85 Agrawal et al. discloses OPC modification to the features which are **non-critical features** (imperfections) (Agrawal et al., column 3, lines 4-5; lines 12-16) by using a **shape-based identification system** (Agrawal et al., column 3, lines 21-22) to perform layout modification. Moreover Agrawal et al. discloses the same shape-based system as instant Application and may be used in any situation requiring identification of layout features (Agrawal et al., column 8, lines 45-48), using the computer system (Figure 11), programming code and conception of using the **shape-based approach**, which enables **accurate** and efficient application of **layout modifications** (Agrawal et al., column 5, lines 51-52), wherein shape-based system described by Agrawal et al. has an ability of distinguishing a level of **"criticality"** (ranking) of shapes to be modified (Agrawal et al., column 7, lines 45-48). Therefore the system disclosed by Agrawal et al. is functioning the same as the system disclosed by Appellants.

Agrawal et al. discloses all limitations of the claims 11, 33, 37, 38, 39, 40, 55, 65, 72, 79, 85

With respect to claims 11 Agrawal et al. discloses a method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality

of polygons (layout features in the first portion) using the **shape-based approach** which enables accurate and efficient application of **layout modifications** (column 14, lines16-19; column 5, lines 51-52; column 8, lines 45-48), the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout by applying the first action to the first set of layout features (column 14, line 31) matching with the **first shape** and the second portion **of the first plurality of properties** (column 14, lines 24-30), the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection wherein the layout features comprises the polygon or groupings of polygons representing the layout imperfection (column14, lines 20-23); the second edge being contiguous with and substantially perpendicular to the first edge as shown on the Figs. 4a, 4b and 4c which provide examples of basic shapes wherein the second edge E412 is contiguous and substantially perpendicular to the first edge E411 (column 6, lines 35-37); and wherein the first shape further comprises: a third edge, the third edge being contiguous with and substantially perpendicular to the second edge as shown o the Figs. 4a-4c, 5a-5d, 6a-6e, 7a-7c and particularly according the Fig. 4b wherein the third edge E423 is contiguous and substantially perpendicular with the second edge E422; a fourth edge, the fourth edge being contiguous with and substantially perpendicular to the third edge as shown o the Figs. 4a-4c, 5a-5d, 6a-6e, 7a-7c and particularly according the Fig. 4c wherein the fourth edge E434 is contiguous and substantially perpendicular with the third edge E433; and a fifth edge, the fifth edge

being contiguous with and substantially perpendicular to the fourth edge as shown o the Figs. 4a-4c, 5a-5d, 6a-6e, 7a-7c and particularly according the Fig. 4c wherein the fifth edge E435 is contiguous and substantially perpendicular with the fourth edge E434 (column 6, lines 44-51; column 17, lines 10-21), wherein none of the first edge, the second edge, the third edge, the fourth edge, and the fifth edge are substantially side-by-side with each other as shown on the Fig. 4c.

With respect to claim 33 Agrawal et al. discloses a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (column 19, lines 25-26; column 20, lines 1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 3-7; lines 20-23); a second set of instructions for performing a first layout beautificati6n action on each of the first set of matching layout features within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 24-25); third set of instructions for defining the first shape according to a set of user inputs within the software wherein any programming code having plurality of sets of code has an ability

of any sequence of having the instructions in the whole code (abstract; column 20, lines 20-22); within the ability of the system and software (programming code) for providing shapes/action as retrieving from a remote source or defining by the user (abstract).

With respect to claim 37 Agrawal et al. discloses a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (column 19, lines 25-26; column 20, lines 1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 3-7); a second set of instructions for performing a first layout beautificati6n action on each of the first set of matching layout features within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 16-19); third set of instructions for defining the first shape according to a set of user inputs within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (abstract; column 20, lines 20-22); a third set of instructions for loading the first shape from across a network within the code processing a first action (first layout beautification action) within the software wherein any programming code

having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 13, lines 51-53; column 20, lines 23-24).

With respect to claim 38 Agrawal et al. discloses a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (column 19, lines 25-26; column 20, lines 1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 3-7); a second set of instructions for performing a first layout beautificati6n action on each of the first set of matching layout features within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 16-19); third set of instructions for defining the first shape according to a set of user inputs within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (abstract; column 20, lines 20-22); a third set of instructions for defining the first layout beautification action according to a set of user inputs within the ability of the system and software (programming code) for providing shapes/action as retrieving from a remote source or defining by the user (abstract).

With respect to claim 39 Agrawal et al. discloses a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (column 19, lines 25-26; column 20, lines 1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 3-7); a second set of instructions for performing a first layout beautificati6n action on each of the first set of matching layout features within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 16-19); third set of instructions for defining the first shape according to a set of user inputs within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (abstract; column 20, lines 20-22); a third set of instructions for loading the first shape from across a network within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code and within the ability of the system and software (programming code)

for providing shapes/action as retrieving from a remote source or defining by the user (abstract; column 13, lines 51-53; column 20, lines 23-24).

With respect to claim 40 Agrawal et al. discloses a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (column 19, lines 25-26; column 20, lines 1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 3-7); a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 16-19); a third set of instructions for comparing a second shape to the plurality of features in each of the plurality of polygons to identify a second set of matching layout features, the second shape comprising at least a third edge and a fourth edge related according to a second property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code and within the ability of the system and software (programming code) for providing shapes/action as retrieving from a remote

source or defining by the user (abstract; column 19, lines 13-19); a fourth set of instructions for performing a second layout beautification action on the second set of matching layout features within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 19, lines 20-24).

With respect to claims 55 Agrawal et al. discloses a method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons (layout features in the first portion) using the **shape-based approach** which enables accurate and efficient application of **layout modifications** (column 14, lines 16-19; column 5, lines 51-52; column 8, lines 45-48), the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout by applying the first action to the first set of layout features (column 14, l.31) matching with the **first shape** and the second portion **of the first plurality of properties** (column 14, lines 24-30), the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection wherein the layout features comprises the polygon or groupings of polygons representing the layout imperfection (column14, lines 20-23).

With respect to claim 65 Agrawal et al. discloses a method for correcting a plurality of layout imperfections in IC layout imperfections in an integrated circuit layout using the **shape-based approach** which enables accurate and efficient application of **layout modifications** (column 14, lines 16-19; column 5, lines 51-52; column 8, lines

45-48), the method comprising: defining a plurality of shapes, each of the plurality of shapes comprising at least a first edge and a second edge related according to at least one of a plurality of defined properties, each of the plurality of shapes matching at least one of the plurality of layout imperfections within a catalog of defined shapes (abstract) comprising a first edge and a second edge coupled (related) in accordance with a first plurality of properties associated with the first shape (column 14, lines 20-23); defining a plurality of actions to correct the plurality of layout imperfections, each of the plurality of actions being associated with at least one of the plurality of shapes within plurality of shapes defined in the catalog of shapes and layout **processing actions** associated with the various shapes (abstract); applying the plurality of actions to the IC layout responsive to the at least one of the plurality of shapes associated with each of the plurality of actions matching elements within the OC layout within applying layout processing actions associated with the various shapes, wherein each layout processing action applies a specified layout **modification** to its associated shape (abstract).

With respect to claims 72 and 79 Agrawal et al. discloses a system for performing layout beautification on an integrated circuit layout data file within a shape-based OPC system 1000 shown on the Fig. 10a including input data file Dfin describing a particular IC layout (column 12, lines 17-18; lines 21-22), the system comprising: an input data manager for loading the IC layout data file into the system using input data manager 1010 shown on the Fig. 10a (column 12, l.19); a layout beautification engine for applying a plurality of corrective actions to the IC layout data file responsive to at least one of a plurality of shapes associated with each of the plurality of corrective

actions matching elements in the IC layout data file, wherein each of the plurality of shapes comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties within the OPC engine 1030 for performing shape matching and action application to the set of plurality of geometries (column 12, lines 49-50), wherein OPC engine 1030 comprises a data controller 1032, a shape scanner 1034 and an action manager 1036 as shown on the Fig. 10b (column 12, lines 51-60); and output data manager for generating an output data file within output data manager 1040 shown on the Fig. 10a (column 12, lines 20-21).

With respect to claim 85 Agrawal et al. discloses a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (column 19, lines 25-26; column 20, lines 1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 3-7; lines 20-23); a second set of instructions for performing a first layout beautificati6n action on each of the first set of matching layout features within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (column 20, lines 24-25).

In Appellants' Appeal brief Appellants' representative states that the passages of Agrawal et al. in the Final Office Action with respect to claims 11, 79, 89 and 96 fail to disclose or suggest the recited layout beautification (action) and layout imperfection. It has to be noted that all passages [the prior art citations] are addressed [mapped] **to the limitations of the claims** (listed above) and accordingly read on them. The limitations of the claims above are silent about layout beautification and layout imperfection. Therefore the instant claims fail to disclose the layout beautification and layout imperfection, since **the preamble is not given the weight of the limitation,** and the layout beautification and layout imperfection language is stated only in the preamble of the claims (see ***IMS Technology v. HAAS Automation INC.*, 54 USPQ2d 1129, 1137 (Fed. Cir. 2000)**).

With respect to claims 33, 37, 38, 39, 40, 55, 72, 85 Appellants have disclosed a definition of **layout beautification** in the Specification at paragraph [0006] as detecting and correcting of layout imperfection. Agrawal et al. discloses **OPC modifications** (column 3, lines 4-5; lines 12-16) **functionally equivalent** to Layout imperfection by "detecting and correcting the same type of layout imperfection" as disclosed by Appellants.

Additionally, Agrawal et al. discloses the same shape-based system as instant Application and may be used in any situation requiring improved identification of layout features (column 8, lines 45-48), using the same computer system (Figure 11), programming code and conception of using the **shape-based approach**, which enables **accurate** and efficient application of **layout modifications** (column 5, lines 51-52),

wherein shape-based system described by Agrawal et al. has an ability of distinguishing a level of "**criticality**" (ranking) of shapes to be modified (column 7, lines 45-48).

Agrawal et al. discloses claims 56, 57, 58, 64

With respect to claim 56 Agrawal et al. discloses the first action comprises adjusting the first type of layout imperfection by a fixed amount as shown on the Fig. 9b wherein a shape S_2 and a modified feature F_2 that could result from application of an action B (beatification process) associated with shape S_2, wherein action narrows and lengthens finger structures matching shape S_2 by a particular amount (column 10, lines 64-67), because shape S_2 was replaced by feature F_2 without dramatically changing the shape of the feature (**beautification of the imperfection**), wherein fixed amount of the of the adjustment might be stored in the bias table, for example table 3 (column 9, lines 6-15).

With respect to claim 57 Agrawal et al. discloses the first type of layout imperfection covers a plurality of actual layout imperfections, each of the plurality of actual layout imperfections having a different set of actual properties, wherein the first action comprises making an adjustment according to the set of actual properties for each of the plurality of actual layout imperfections within plurality of shapes wherein each shape having set of properties and layout processing actions are based on the properties (column 3, lines 24-26; column 6, lines14-18) and wherein each shape represents a type of features and shapes are grouped based on associated edges and the property associated with the group of shapes; using the conception of the shape-based approach to apply more accurate/appropriate corrections to IC layout features

(column 6, lines 57-58), wherein shape-based system described by Agrawal et al. has an ability of distinguishing a level of "**criticality**" (ranking) of shapes to be modified (column 7, lines 45-48).

With respect claim 58 Agrawal et al. discloses the first action comprises replacing the first type of layout imperfection with a second shape within the catalog of shapes specifying actions as functions of the property variables of the shapes (column 8, lines 37-39; column 10, lines 34-36); wherein the shape-based system may be used in any situation requiring **improved identification** of layout features (column 8, lines 45-48) using processing the catalog of shapes and applying the **appropriate actions to all matches layout features** (column 10, lines 38-41).

With respect to claim 64 Agrawal et al. discloses the second edge being contiguous with and substantially perpendicular to the first edge as shown on the Fig. 6d, wherein the entire collection of edges 661-673 as a single shape (column 7, lines 65-67; column 8, lines 1-2) and the first edge 661 is contiguous with and substantially perpendicular to the second edge 662; wherein the first shape further comprises: a third edge 663, the third edge being contiguous with and substantially perpendicular to the second edge 662, wherein the third edge 663 is not substantially side-by-side with the first edge 661; a fourth edge 664, the fourth edge 664 being contiguous with and substantially perpendicular to the third edge 663, wherein the fourth edge is not substantially side-by-side with the second edge 662; a fifth edge 665, the fifth edge 665 being contiguous with and substantially perpendicular to the fourth edge 664, wherein the fifth edge is substantially parallel to and side-by-side with the third edge 663; a sixth

edge 666, the sixth edge 666 being contiguous with and substantially perpendicular to the fifth edge 665, wherein the sixth edge is not substantially side-by-side with the fourth edge 664; and a seventh edge 667, the seventh edge being contiguous with and substantially perpendicular to the sixth edge, the seventh edge being substantially parallel to and side-by-side with the first edge. Appellant's representative states that cited shape 660 in Figure 6d of Agrawal et al. reference (including plurality of edges) fails to teach limitations of the claim 64. Examiner disagrees. The limitations of the claim 64 satisfy the Figure 6d and its description having plurality of edges being configured in the way described in the Figure 6d.

Agrawal et al. discloses claim 67

With respect to claim 67 Agrawal et al. discloses the specified sequence being determined according to a predefined ranking of layout imperfection criticality within the shape-based OPC system applying different bias features to the photomask layout for features (column 5, lines 64-67) wherein shape-based system described by Agrawal et al. has an ability of distinguishing a level of "**criticality**" (ranking) of shapes to be modified (column 7, lines 45-48).

Agrawal et al. discloses claim 73

With respect to claim 73 Agrawal et al. discloses the IC layout data file comprises a fractured data file within a definition of a fracturing operation which is comprised in the first action being to match the first shape which is stored in the catalog of shapes (column 18, lines 56-59), which is included into a input data file Dfin, and wherein loading the IC layout data file into the system comprises reassembling a plurality of

layout primitives into a plurality of polygons (column 8, lines 42-44; column 12, line 57) and wherein input data manager 1010 divides data file Dfin into its various layers and discrete sets of geometries within each layer (column 12, lines30-32); wherein data manager 1010 shown on the Figure 10a **divides data file into discrete sets** of **geometries**, wherein set of geometries might only include only single polygon (column 12, lines 30-35).

Agrawal et al. discloses claims 89, 91, 96, 99

With respect to claim 89 Agrawal et al. discloses an apparatus for reducing output data size in an input layout by beautifying the input layout by the system shown on the Fig. 11 including forming a grouping substantially similar in size and configuration to feature as shown on the Fig. 3a (column 5, lines 59-61), the apparatus comprising: means for identifying a shape pattern in the input layout, wherein the shape pattern comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties (column 14, lines 20-24); and means for replacing the identified shape pattern with an alternative configuration, the alternative configuration reducing data volume by using a "wildcard" that allows the shape to identify a range of actual layout features as shown on the Fig. 7d (column 8, lines 18-21); the alternative configuration provides one of and absolute correction, an adaptive correction, and a replacement correction by using model-based actions, when fixed value adjustment is made, rule-based actions, when adjustment depends on actual characteristics, and shape-based actions, when action with replacement shapes respectively (abstract). Moreover data manager 1010 shown on the Figure 10a **divides data file into discrete**

sets of **geometries**, wherein set of geometries might only include only single polygon (column 12, lines 30-35) and processing the data along with hierarchy manager 1020 organizing and categorizes the sets of geometries according to a predefined ordering basis **to minimize the amount of data** (column 12, lines 41-44), using the conception of **selectively preventing or allowing bias** application in the regions (column 11, lines 35-36).

With respect to claim 91 Agrawal et al. discloses a method of providing corrective actions to a layout based on shape analysis using the shape-based approach which enables accurate and efficient application of layout modifications (column 14, lines 16-19; column 5, lines 51-52; column 8, lines 45-48), the method comprising: identifying shape patterns on the layout, wherein each shape pattern comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties (column 14., lines 20-23); modifying the layout according to corrective actions associated with the identified shape patterns, thereby removing at least one layout imperfection, wherein the corrective actions using the shape-based system for layout modification (column 8, lines 45-48) include at least one of: performing a first operation using a fixed value associated with an existing layout parameter of an identified shape pattern as applying rule-based OPC (column 4, line 49); performing a second operation that is a function of an existing layout parameter of an identified shape pattern as a model-based OPC actions (column 4, line 50); performing a third operation that replaces an identified shape pattern as a filler-shapes (column 4, lines 45-48). Moreover

the process described by the Figure 9b replaces the old shape by a new shape **removing imperfection (S_2) from the layout** (column 10, lines 64-67).

With respect to claims 96 Agrawal et al. discloses a shape-based beautification method in a layout using the shape-based approach which enables accurate and efficient application of layout modifications (column 14, lines 16-19; column 5, lines 51-52; column 8, lines 45-48), the method comprising: identifying a shape pattern on the layout (column 14, lines 20-23); and applying at least one of an absolute correction using a fixed value associated with an existing layout parameter of an identified shape pattern as applying rule-based OPC (column 4, l.49), an adaptive correction as a model-based OPC actions (column 4, l.50), and a replacement correction to the identified shape pattern as a filler-shapes (column 4, lines 45-48), thereby removing at least one layout imperfection and reducing fracturing data volume in the layout wherein the corrective actions using the shape-based system for layout modification (column 8, lines 45-48) and dividing input data Dfin into its various layers and discrete sets of geometries within each layer (column 12, lines 31-37). Moreover data manager 1010 shown on the Figure 10a **divides data file into discrete sets** of **geometries**, wherein set of geometries might only include only single polygon (column 12, lines 30-35) and processing the data along with hierarchy manager 1020 organizing and categorizes the sets of geometries according to a predefined ordering basis **to minimize the amount of data** (column 12, lines 41-44), using the conception of **selectively preventing or allowing bias** application in the regions (column 11, lines 35-36), wherein the process,

described by the Figure 9b, replaces the old shape by a new shape **removing imperfection (S_2) from the layout** (column 10, lines 64-67).

With respect to claim 99 Agrawal et al. discloses the replacement correction replaces the identified shape pattern with a simplified shape pattern as shown on the Fig. 9b wherein a shape S_2 and a modified feature F_2 that could result from application of an action B (beatification process) associated with shape S_2, wherein action narrows and lengthens finger structures matching shape S_2 by a particular amount (column 10, lines 64-67), because shape S_2 was **replaced** by feature F_2 without dramatically changing the shape of the feature (**beautification of the imperfection**), i.e. the **imperfection** was removed.

Conclusion

Having considered all Appellants' arguments, Examiner maintains that the Agrawal et al. discloses the limitations of Appellants' claims. For the above reasons, it is believed that the rejections of the claims 11, 33, 37-43, 55-99 under 35 U.S.C. § 102(e) should be sustained.

Respectfully submitted,

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